REMARKS

STATUS OF THE CLAIMS

Claims 1-6, 13-18, 20-22, 24-28 and 32 have been pending in the application.

Claims 2-6, 20-22 and 24-28 are allowed.

The Office Action page 9, item 21 objects to claims 15-16 for being allowable if amended into independent form.

Claims 13, 14 and 17 are rejected under 35 USC 102(e) as being anticipated by Hartnett (US 6,167,479).

Claims 13, 14 and 17 are rejected under 35 USC 103(a) as being unpatentable over Hartnett in view of Helsch (US Patent No. 5,774,724).

Claim 32 is rejected under 35 USC 103(a) as being unpatentable over Hartnett in view of Takano (US Patent No. 5,070,473).

Claim 32 is cancelled without prejudice or disclaimer, rejected claims 13-18 are amended, and, thus, rejected claims 13-18 remain pending for reconsideration, which is respectfully requested.

No new matter has been added.

REJECTION

The pending rejected independent claim is 17. Claim 14 is amended as independent form and is directed to 2nd, 3rd, 4th, and 5th embodiments (see the present Application page 66, line 5+). Amended dependent claims 13 and 15 are directed to the 2nd embodiment. Amended dependent claims 15, 17 and 18 are directed to the 3rd, 4th and 5th embodiments, respectively.

The claimed present invention is clarified as follows: Generally, an interrupt occurs immediately after an error (e.g., overflow, underflow, etc.) occurs during execution of an instruction. However, when the instruction is some kind of MOP ("M" means media; MOPs are instructions for real-time image processing, for example), program execution might not be interrupted and subsequent instructions are executed, because the error might only cause noise. In other words, in a real-time image processing, processing speed has priority over image quality. However an error of other kinds of MOPs should be corrected on the spot, because it

may affect the execution result of subsequent instructions. According to the 2nd to 5th embodiments of the present invention, when an error is detected, the occurrence of an error is written into the MSR (e.g., a Media Status Register 267 in FIG. 13) without interrupting program execution, and afterwards, more specifically, when an interruption occurs, it is determined whether to check the MSR to perform the error correction processing if any error has been detected.

Hartnett relates to testing interrupt control and processing logic and column 3, lines 36-40 discuss "... a system for selectively injecting errors within the instruction stream of a data processing system." Heisch relates to processor performance monitoring and column 3, line 63 to column 4, line 38 discuss "... an instruction address breakpoint may be set for any effective address in a program utilizing an instruction address breakpoint register (IABR)."

However, Hartnett and Heisch fail to disclose or suggest to one skilled in the art the claimed present invention as recited in amended independent claim 14:

> 14. (CURRENTLY AMENDED) ~~The exception processing method according claim 17, further comprising~~ An exception processing method for a processor that executes a program including a first instruction and a second instruction, and that performs, after an interruption caused by the second instruction and before execution of interrupt processing, exception processing for an exception that has occurred during execution of the first instruction, wherein the first instruction is a specific application-purpose operation instruction, the exception processing method comprising:
>
> ***setting, when the exception occurs during the execution of the first instruction, a value indicating occurrence of the exception*** in a register or a flag (e.g., specific application purpose operation status register 267 shown in FIGS. 13, 20, 22 and 25);
>
> determining (steps 509&510, 607&608, 707&708, 907&908, 1507&1508, and 1607&1608 shown in FIGS. 17, 18, 19, 21, 24, 27 and 28) when the ***interruption is caused by the second instruction, whether the exception has occurred by reading the register or the flag;***
>
> ***performing (steps 511, 609, 709, 1209, 1509, 1609 shown in FIGS. 17, 18, 19, 21, 24, 27 and 28) the exception processing for the first instruction, if the exception has occurred according to the reading of the register or the flag;*** and
>
> ***performing the interrupt processing for the second***

> ***instruction*** *(steps 504, 604, 704, 904, 1204, 1504, 1604 shown in FIGS. 17, 18, 19, 21, 24, 27 and 28)* ***to return from the interruption*** *(steps 506, 606, 706, 906, 1206, 1506, 1606 shown in FIGS. 17, 18, 19, 21, 24, 27 and 28*~~storing a value, which indicates the detection of the operation exception during the execution of the specific application purpose operation instruction, in a memory, and confirming whether an operation exception has been detected or not by referring to the content of said memory~~.

Further, in contrast to Harntett and Heisch, if determined that an exception has occurred based upon reading the set register or flag, the dependent claims provide conditions based upon which an exception processing for the first instruction should be performed. For example, dependent claims 15 provides:

> 15. (CURRENTLY AMENDED) The exception processing method according to ~~claim 17~~claim 14, further comprising:
>
> determining (steps 502&503, 602&603, 702&703 of FIG>S 17, 18 and 19) before the execution of the exception processing (steps 511, 609, 709 of FIGS. 17, 18 and 19), whether to perform the exception processing by reading a second register or a second flag (operation mode register 268 shown in FIG. 13) that stores an operation mode indicating to the processor whether to perform the exception processing~~storing a value in a register or a flag indicating that the operation state has been set to a state where the operation exception, which occurs during the execution of a specific application purpose operation instruction, is detected, and~~
>
> ~~confirming whether the operation state has been set to the state where the operation exception is detected by referring to said register or said flag~~.

In view of the claim amendments and remarks, withdrawal of the rejection of pending claims and allowance of pending claims is respectfully requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Respectfully submitted,
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